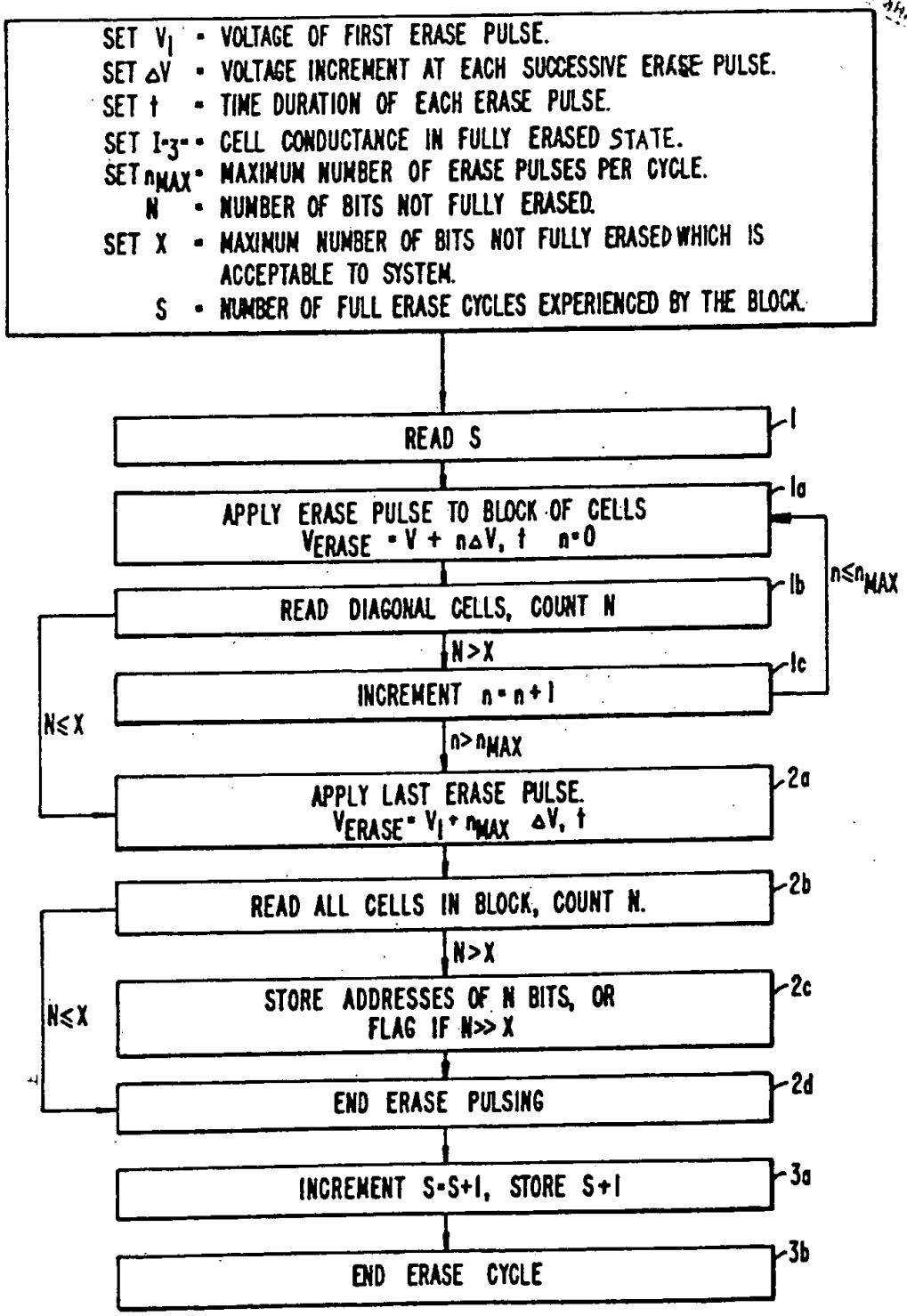
SET V_1 = VOLTAGE OF FIRST ERASE PULSE.
SET ΔV = VOLTAGE INCREMENT AT EACH SUCCESSIVE ERASE PULSE.
SET t = TIME DURATION OF EACH ERASE PULSE.
SET I_{-3} = CELL CONDUCTANCE IN FULLY ERASED STATE.
SET n_{MAX} = MAXIMUM NUMBER OF ERASE PULSES PER CYCLE.
N = NUMBER OF BITS NOT FULLY ERASED.
SET X = MAXIMUM NUMBER OF BITS NOT FULLY ERASED WHICH IS ACCEPTABLE TO SYSTEM.
S = NUMBER OF FULL ERASE CYCLES EXPERIENCED BY THE BLOCK.
READ S
1
APPLY ERASE PULSE TO BLOCK OF CELLS
$V_{ERASE} = V + n\Delta V$, t n=0
1a
READ DIAGONAL CELLS, COUNT N
1b
N>X
INCREMENT n = n+1
1c
$n \leq n_{MAX}$
N≤X
$n > n_{MAX}$
APPLY LAST ERASE PULSE.
$V_{ERASE} = V_1 + n_{MAX}$ ΔV, t
2a
READ ALL CELLS IN BLOCK, COUNT N.
2b
N>X
N≤X
STORE ADDRESSES OF N BITS, OR FLAG IF N>>X
2c
END ERASE PULSING
2d
INCREMENT S=S+1, STORE S+1
3a
END ERASE CYCLE
3b

FIGURE 9

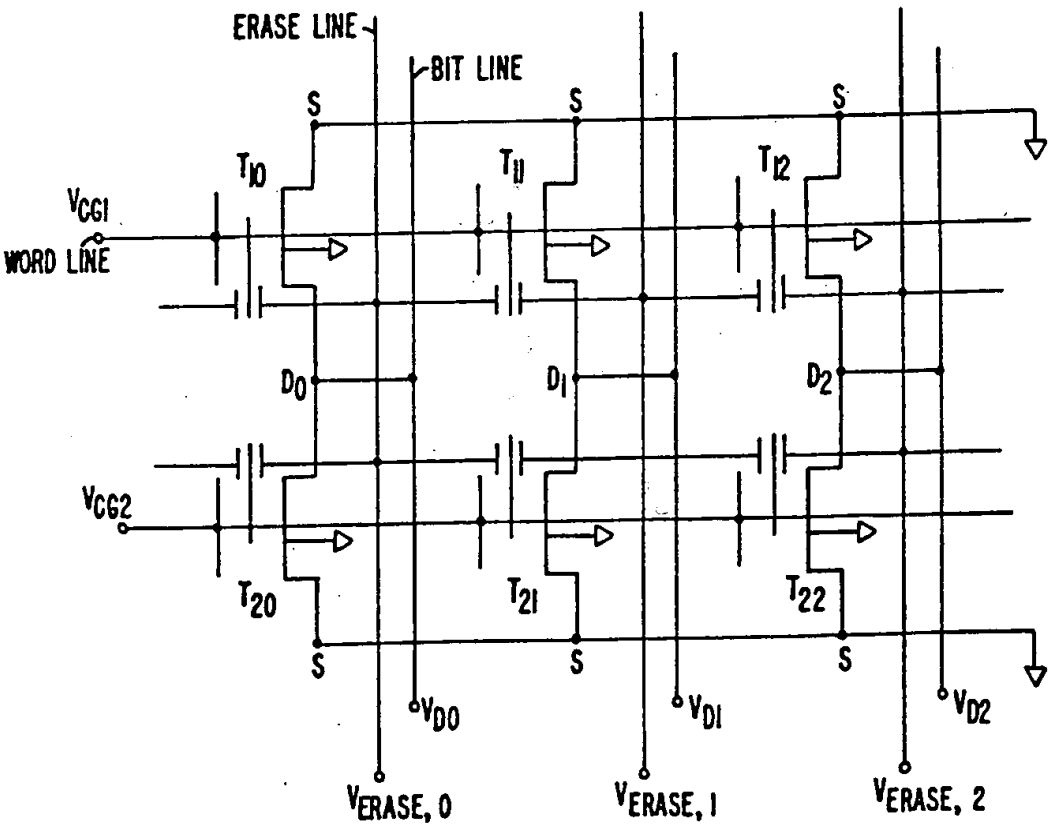
ERASE LINE
BIT LINE
S
S
S
T_{10}
T_{11}
T_{12}
V_{CG1}
WORD LINE
D_0
D_1
D_2
V_{CG2}
T_{20}
T_{21}
T_{22}
S
S
S
V_{D0}
V_{D1}
V_{D2}
$V_{ERASE,0}$
$V_{ERASE,1}$
$V_{ERASE,2}$

FIGURE 10

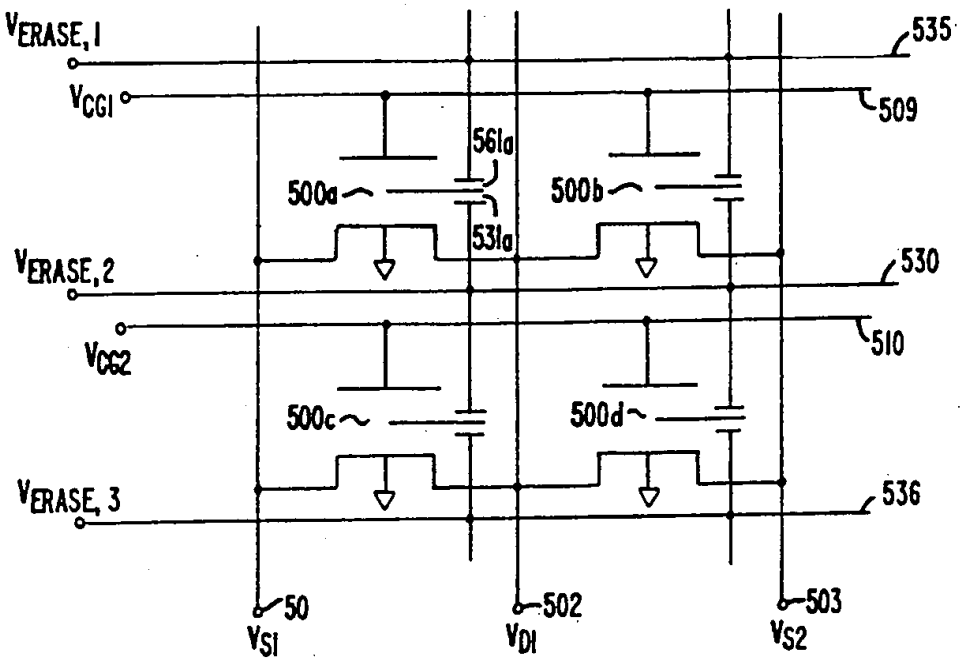
VERASE, 1
535
VCG1
509
561a
500a
500b
531a
VERASE, 2
530
VCG2
510
500c
500d
VERASE, 3
536
50
502
503
VS1
VD1
VS2

FIGURE 11

TABLE I. ARRAY OF FIGURE 10

	V_{CG}			V_D			S			V_{ERASE}		
	SEL. CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL		SEL CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL	
		SAME ROW	SAME COL.		SAME ROW	SAME COL.		SAME ROW	SAME COL.		SAME ROW	SAME COL.
READ	5V	5V	0V	1.5V	0V	1.5V	0V	0V	0V	0V	0V	0V
ERASE	0V	0V	0V	0V	0V	0V	0V	0V	0V	20V	20V (BLOCK	20V ERASE)
PROGRAM	12V	12V	0V	8V	0V	8V	0V	0V	0V	0V	0V	0V

FIGURE 12

TABLE II. VIRTUAL GROUND ARRAY OF FIGURE 11

	V_{CG}			V_D			S			V_{ERASE}		
	SEL. CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL		SEL. CELL	UNSEL. CELL	
		SAME ROW	SAME COL.		SAME ROW	SAME COL.		SAME ROW	SAME COL		SAME ROW	SAME COL.
READ	5V	5V	0V	1.5V	1.5V	1.5V	0V	1.5V	0V	0V	0V	0V
ERASE	0V	0V	0V	0V	0V	0V	0V	0V	0V	20V	20V (BLOCK	20V ERASE)
PROGRAM	12V	12V	0V	8V	FLOAT	8V	~0V	FLOAT	~0V	0V	0V	0V

FIGURE 13